

## REMARKS

This Response to Office Action is responsive to the Office Action from the Examiner mailed February 23, 2006. Reconsideration and withdrawal of the rejections set forth in the Office Action is respectfully requested. The applicants have amended claims 36, 39, and 40. The applicants have added new claims 50-57. Claim 36 is distinguished from the prior art and dependent claims 50 and 51 have been added as a particular commercial embodiment which further distinguish and require no new search to examine. Claims 52-57 closely parallel claim 35 and require no new search to examine. No new matter has been added. Applicant thanks the Examiner for the careful review of this application. Claims 36-56 remain pending in this application.

### Rejection under 35 U.S.C. § 103(a)

Claims 36-39 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,272,153 to Huang et al. (hereinafter "Huang").

Claims 40-44 and 47 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Huang in view of U.S. Patent No. 6,449,519 to Kuwaoka (hereinafter "Kuwaoka").

Claims 45-46 and 48-49 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Huang as modified by Kuwaoka in further view of U.S. Patent No. 6,233,562 to Sueyoshi et al. (hereinafter "Sueyoshi").

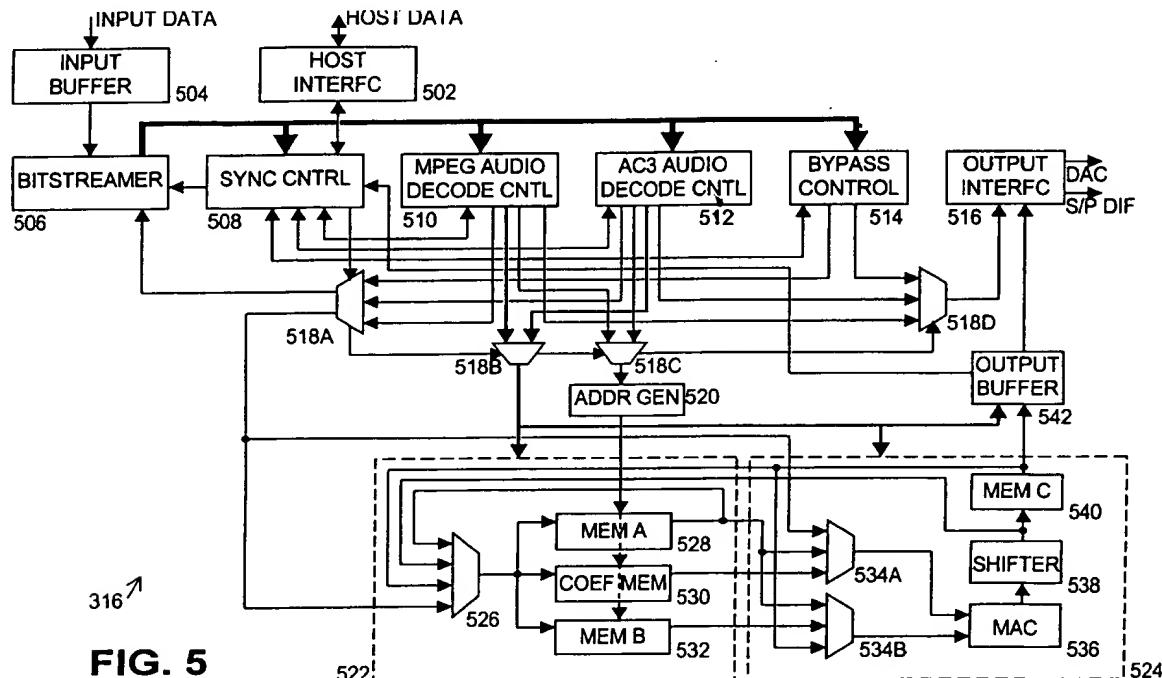
Two Month Extension – Pursuant to 37 C.F.R. 1.136(a), the Applicants hereby petition for a two-month extension of time to respond to the Office Action. This extension will extend the response due date to Monday, July 24, 2006.

### Prior Art

Huang teaches an audio decoder architecture that uses various component sharing techniques to conserve hardware and reduce implementation costs. [Huang, col. 2, lines 27-30]. Huang teaches an audio decoder comprises a host interface, an input buffer, a bitstream, a synchronization controller, an MPEG audio decode controller, an AC3 audio decode controller, a bypass controller, an output interface, a set of controller multiplexers, an address generator, a memory module, a data path module, and an output buffer.

[Huang, col. 7, lines 32-42] The host interface 502 is coupled to the sync controller 508.

[Huang, col. 7 line 45, Fig.5] Figure 5 has been reproduced for convenience below:



**FIG. 5**

The host interface 502 communicates read and write status and configuration information to registers in the sync controller 508. [Huang, col. 7, lines 46-48, Fig. 5] Moreover, the input buffer 504 is coupled to the bitstreamer 506 which is coupled to the sync controller 508. [Huang, Fig. 5] At the beginning of each audio data frame, the sync controller 508 is in control of the bitstreamer 506. [Huang, col. 8, lines 8-10, Fig. 5] The sync controller 508 parses the audio data frame headers and extracts audio data format information and uses the audio data format information to determine the data type. [Huang, col. 7, line 66 – col. 8 line 8, Fig. 5] Once the sync controller 508 extracts the audio data format information, a set of multiplexers 518, controlled by the sync controller 508, routes the data to one of three decode/controllers 510, 512, 514 to decode the audio signal. [Huang, col. 8, lines 19-28, Fig. 5] The three decode/controllers include an MPEG audio decode controller 510, an AC3 decode controller 512, and a bypass control 514. [Huang, Fig. 5] The MPEG audio decode controller 510 and the AC3 audio decode controller 512 decode the audio data compressed according to the corresponding standard while the

bypass control 514 operates to bypass the decoding process and forwards the information to the output buffer. [Huang, col.8, lines 13-19, Fig. 5]

Kuwaoka teaches a harmonic generation circuit allowing audio information in a narrow frequency band can be converted into audio having a wide frequency band using a low-price circuit arrangement. [Kuwaoka, col. 2, lines 46-49] Kuwaoka teaches comparing audio data subjected to a delay corresponding to one sample by the delay circuit used to output a comparison between top-peak and under-peak and under-peak and top-peak. [Kuwaoka, col.8, lines 31-42] The harmonic generation circuit uses the comparisons to select a pattern. [Kuwaoka, col. 8, lines 43-51]

### **Prior Art Distinguished**

Claim 36 was rejected as unpatentable by Huang under Section 103(a) and has been amended to include the language "by analyzing the associated clock signal". In Huang the audio data format is determined by parsing the audio data frame headers and extracting bitstream side information [Huang, col. 7, line 66 – col. 8, line 2]. Huang does not teach analyzing the associated clock signal to determine the audio data format, as illustrated by the excerpt below:

"Sync Controller 508 implements a state machine for parsing the audio data frame headers and extracting bitstream side information (BSI) such as audio data format ... the sync controller is 508 is written to accommodate the variations in header field formats due to the various supported audio data format" [Huang, col. 7, line 66 – col. 8, line 8]

Therefore, Huang does not render Claim 36 unpatentable. For at least these reasons, the independent Claim 36 is allowable over the teachings of Huang.

Claim 36 is patentable over Huang in light of Kuwaoka. Kuwaoka teaches using peak comparisons to select a pattern. [Kuwaoka, col. 8, lines 43-46] Kuwaoka does not teach nor suggest audio format detection "by analyzing the associated clock signal". Kuwaoka teaches comparing audio data subjected to a delay corresponding to one sample by the delay circuit used to output a comparison between top-peak and under-peak and

under-peak and top-peak, and not the analysis of a clock signal. [Kuwaoka, col.8, lines 31-42]

For a prima facie 35 U.S.C. 103(a) obviousness rejection, "all the claim limitations must be taught or suggested by the prior art". [MPEP, 2143.03] Since the cited prior art does not teach nor suggest every aspect of claim 36, claim 36 is allowable over the cited prior art.

Claims 37-49 are either directly or indirectly dependent on the independent Claim 36. As described above, the independent Claim 36 is allowable over the teachings of Huang. Accordingly, Claims 37-49 are also at least allowable as being dependent on an allowable claim. New claims 50-56 are allowable for similar reasons as claims 36-49.

Applicant respectfully submits that discussion of Sueyoshi is unnecessary in light of the above arguments as the claims are patentable over the teachings of Huang and are in condition for allowance.

**CONCLUSION**

In view of the foregoing, Applicants submit that the claims pending in the application patentably define over the prior art. A Notice of Allowance is therefore respectfully requested.

If in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is encouraged to call the undersigned at (650) 838-4307.

Respectfully submitted,  
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